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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/385,014	08/27/1999	NAOHARU SHINOZAKI	P8075-9014	8603
7590	01/13/2005		EXAMINER	
ARENT FOX KINTNER PLOTKIN & KAHN PLLC 1050 CONNECTICUT AVENUE, N.W. SUITE 400 WASHINGTON, DC 20036-5339			LE, DINH THANH	
			ART UNIT	PAPER NUMBER
			2816	

DATE MAILED: 01/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/385,014	SHINOZAKI, NAOHARU
	Examiner	Art Unit
	DINH T. LE	2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

**A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM
 THE MAILING DATE OF THIS COMMUNICATION.**

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 03 May 2004.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1,2 and 4-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1,2 and 4-21 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
 If approved, corrected drawings are required in reply to this Office action.
- 12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
 a) The translation of the foreign language provisional application has been received.
- 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|--|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ . |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ . | 6) <input type="checkbox"/> Other: _____ . |

NON-FINAL REJECTION

Response to Applicant's Amendment

Claims Rejections

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-2, 4-5 and 16-21 are rejected under 35 USC 103(a) as being unpatentable over Takahashi et al (JP40927070).

Takahashi et al teaches an amplifier circuit in Figures 1-5 comprising a differential circuit (N3, N4, P3, P4), a current regulating circuit (P2, N6), a constant current source (P1, N5) and a even number of feedback delay elements (inverters V1, V3-V5) but does not disclose the limitation "the regulating circuit current increases an amount of the current flowing through the differential circuit to be increase in response to the node signal when the first transistor changes its state from an activated state in response to an external signal, such that only rising delay time of the node signal is shortened". For example, the circuits in Figures 1 and 4 of Takashi have the structure similar to the claimed circuit as shown in Figures 6-7 of the present invention with exception of that Takashi employs fourth feedback delay elements (V1, V3-V4) instead of one feedback delay element (5) as shown in the present invention. In order to meet the above recited limitation, only one inverter must be used in the circuit of Takahashi et al. However, a skilled

artisan recognizes that the feedback signals in the circuit of Takashi is to used to provide a predetermined delay for activating/deactivating the current regulating circuits (P2, N6) and the speed cycle time of the amplifier device is determined by the number of the feedback delay elements, see the Abstract. Since the number of the feedback delay elements is selectable, selecting the number of feedback delay elements of Takahashi et al for providing a predetermined speed cycle time required by a predetermined system in which the circuit of Takahashi et al is to be used is considered to be a matter of a design expedient for an engineer. It would have been obvious to a person having skill in the art at the time the invention was made to select one feedback delay element for the circuit of Takahashi et al for the purpose of increase the speed cycle time of the amplifier. Noted that the regulating circuit current (P2, N6) of the modified circuit of Takashi et al including one selected inverter would "increases an amount of the current flowing through the differential circuit to be increase in response to the node signal when the first transistor changes its state from an activated state in response to an external signal, such that only rising delay time of the node signal is shortened" as claimed.

Claims 6-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Figure 1 of the applicant's admitted prior art in view of Takahashi et al (JP40927070).

Figure 1 of the admitted prior art shows a circuit comprising the amplifier (2a), and a processing signal circuit or a latch circuit (3) but does not discloses that the amplifiers have a current regulating circuit increases an amount of the current flowing through the differential circuit in response to the node signal such that only rising delay time of the node signal is shortened". Takahashi et al teaches a modified amplifier circuit as discussed above. It would have been obvious to a person having skill in the art at the time the invention was made to

employ the modified amplifier circuit taught by Takahashi et al in the circuit of the admitted prior art for the purpose of increase the speed of cycle time. Note that, as notoriously well known in the art, the latch circuit or the processing signal circuit of the admitted prior art can be duplicated to provide more output signals. Thus, duplicating the latch circuit of the circuit of the admitted prior art is a common practice for an engineer is considered to be a matter of the design expedient for the engineer depending upon a particular application. See *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8. Noting that the phase difference between the output signal and the output signal of Takahashi et al is adjustable using the inverters. Therefore, adjusting the output phase same as the input phase for a particular environment would have been obvious to a person having skill in the art.

Response to Applicant's Arguments

The applicant argues that Takahashi fails to disclose the current regulating circuit that conditions an amount of the current flowing through a differential circuit to be increased in response to a node signal when a first transistor changes its state from an activated state to an deactivated state in response to an external signal, such that only a rising delay time of the node signal is shortened. For example, Takahashi et al fails to condition an amount of the current flowing through a differential circuit to be increased when a first transistor (P3; N3) changes its state from an activated stat: to a deactivated state. Specifically, in Figs. 1 and 2 of Takahashi, a transistor P2 operated to increase an amount of current after a transistor P3 is deactivated in response to a rising edge of an input signal Vin, boosting a voltage of a node from a low level by AV to shorten a rising delay time of a node signal when the input signal Vin falls. The

arguments are not persuasive because the modified circuit of Takahashi et al with one selected inverter would cause the regulating circuit current (P2, N6) to increase an amount of the current flowing through the differential circuit to be increase in response to the node signal when the first transistor changes its state from an activated state in response to an external signal, such that only rising delay time of the node signal is shortened” as claimed.

The applicant argues that reducing the number of the inverters in the circuit of Takahashi et al may not operate in a manner as claimed. The argument is not persuasive. As shown in Figures 1-5, the circuit of Takahashi et al. has the structure similar to the structure of the claimed circuit with the exception of the amount of the inverters being used in the feedback loop for adjusting the cycle time of the output signal. Thus, employing one inverter in the circuit of Takahashi for the purpose of increasing the cycle time for accommodating with the requirement of a predetermined system in which the modified circuit of Takahashi et al is to be used would have been obvious and is considered to be a matter of a design expedient for an engineer. Obviously, the modified circuit of Takahashi et al with one selected inverter would operate in the same manner as the claimed circuit since both circuits have the same structure.

CONCLUSION

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DINH T. LE whose telephone number is (571) 272-1745. The examiner can normally be reached on Monday-Friday (8AM-7PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY CALLAHAN can be reached at (571) 272-1740.

Art Unit: 2816

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



DINH T. LE
PRIMARY EXAMINER